MARCELO SIERO

INNERVISION COMPUTERS/IDEASSIERO
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Mr. Siero brings 30 years of a broad base of experience in computer engineering and technical marketing. He was in the team that successfully designed and launched to market the very first VLSI HP3000 computer for Hewlett Packard Corporation. He worked at Xerox PARC during the early revolution of the computer industry in the design of a VLSI bit-mapped display computer processor. He pioneered and ran an Internet Service Provider Business for 9 years in the early 90's. He created a Computer Aided Design infrastructure for the logical verification of a family of very large scale (20-40M transistors) SPARC microprocessors. He has founded and provided the technical infrastructure support for several socially-conscious businesses in the connected world of the 21st Century. Visit www.ee.com for more details.

AREAS OF EXPERTISE

Computer and VLSI Design, and Computer Design CAD

- Design verification: functional, logic, circuit, and layout.
- CISC and RISC computer architecture definition, including hardware and software.
- Implementation of computer farms for computer simulation applications
- Digital design VLSI/board level, circuit design, testing
- Bit-slice systems and microprogramming
- Computer bit-map graphics and video systems
- use of SPICE, DRC/LVS checking, logic simulators, and schematic capture systems.

Software Development

- Linux based software development, C++ and Perl based.
- 32-bit microprocessors: Intel x86 and i860, NSM 32000, AMD 29XXX, Gmicro/100/200/300,(TRON), IBM RS/6000, Fujitsu Sparclite, MIPS R3000/4000, Motorola 68040.
- Gnu compiler-based embedded software development.
- Embedded processor hardware design.

Compiler Design and Software Development

- C, C++, Pascal compilers, design and development
- Code generation and optimization techniques, including data flow analysis
- Operating systems administration: Linux

Technical Documentation and Instruction

- Technical documentation: software, hardware, VLSI CAD, computer technology.
- Languages and other software tools: Perl, C++, Pascal, CGI + much more.
- Technical Training, Unix, Perl and other subjects

Internet Infrastructure Management

- Internet server deployment and management under Linux
- Security and system administration under Linux
- Perl + CGI web-based programming
- MySQL web database programming

SAMPLER OF CLIENTS AND PROJECTS
for InnerVision Computers

Montalvo Systems

Montalvo Systems is a well funded fabless semiconductor startup funded by prominent Silicon Valley V.C. firms.

Spice Navigator:

Developed a system for navigating large SPICE files and providing a computer assisted system for creating timing measurements in hierarchical and RC extracted models. This program also served as a powerful library to manipulate netlist within other tools.

Developed a donut maker program to provide accurate timing while dramatically reducing the size of circuits involving large arrays of cells.

Provided tools to facilitate with the generation of patterns for SPICE simulation across multi-ported macros.

HAL Computers

HAL was one of the largest start-ups in Silicon Valley which later became a wholly owned subsidiary of Fujitsu. Its charter was to make very high-end high performance 64-bit SPARC processors. This contract spanned a period of eight years, ending in the year 2000. Innervision's contract was by far the longest standing contract awarded to a private consulting firm in the history of HAL. The work performed provided tools that became the the workhorse for verification and bring-up (JTAG based) for their state-of-the-art microprocessors for many years. The tools also evolved in being used for bring-up of these processors as well.

LDB – Logic Debugger System:

Conceived and developed a new paradigm for design verification of advanced computer architectures. The system implemented became widely used as the foundation for the verification platform used to test all models of VLSI processors developed at HAL. This system connected a variety of simulation platforms that HAL used to verify their microprocessors, including: a

functional simulator and numerous different types of logic simulators such as Verilog VCS, and Hal's own Aida simulator. Additional facilities were added for implementation of a logic to functional design comparator.

LDBRUN – Redundant Integrated Load-balancing Verification Platform:
Designed and developed a platform for the integration and load balancing of thousands of verification jobs on a farm of 500 networked computers. The system launched test jobs and collected and integrated test results. The system also detected failed jobs and provided redundant relaunching of jobs as needed to guarantee unsupervised results for overnight runs.

LDB/TISIM: Logic Debugger for Physical Hardware Bring up:
LDB was also extended to interface with a JTAG interface allowing the probing and setting the entire internal state of the processor. This tool became the primary vehicle used in the bring-up lab, to get bring the processors to life.

Both LDB and LDB/TISIM were built by creating a customized version of the PERL language, which made its use suitable for hardware simulation applications.

In addition there was a large variety of projects in the area of timing verification, logic verification and IC layout.

Houses.com and Artists.com

Led a small team to design, implement and support the infrastructure for these sites, all the way from artistic design, to web site implementation, hosting and IT infrastructure and security. Coding was implemented in: HTML, CSS, Javascript, Perl CGI, PHP, and MySQL, with assistance from Photoshop Creative Suite, Macromedia Dreamweaver and Flash.

SPEC

Porting of SPEC Benchmarks from Unix to Windows/NT (using Perl, C shell and Make programs).

Intel

Development of BAPCO benchmark management system, both a DOS and a Windows 3.1 version. Neither are Intel released products, and are getting extensive use in the industry. They were developed using Borland's Object Windows Library and C++.

Writing of Instruction set description chapter for *80386 Microprocessor Reference Manual* including development of new notation and algorithmic description for instruction. The Instruction set description has been used in subsequent X86 instruction set manuals even onto present day.

Writing of chapter 1,2 and 3 of *i860 Microprocessor Hardware Manual.*

Infoserv Connections

Development of Windows-based email and newsreader program for operation on both LAN's and WAN's. This feature packed software suite possessed many features similar to Eudora and Microsoft Outlook. This was the first of such programs to include a very powerful newsreader system, use of the right

mouse button, and implement MIME attachments. This served as the foundation for a highly reliable e-mail service spanning a period of seven years.

Fujitsu

Benchmarking of systems and embedded processors involving: Gmicro/200/300, AMD 29XXX, Motorola 680X0, SPARC, MIPS, as well as Vector Processing/RS6000 numerical performance studies based on Livermore Benchmarks. Analyze compiler code optimizations and architectural issues. C and C++ compiler functional testing and optimizer evaluation. Projects involved use of Gnu, MRI and Greenhill's compilers.

Mitsubishi

Cost/performance surveys of microprocessors and BitBlt graphics performance study.

SEIU

Development and Installation of Member Tracking System based on Paradox for Windows/Object PAL on LANTASTIC network.

InnerVision

Assembler and linker development for NS32000 dual processor system. Neural-net pattern recognition system.

JPL

VLSI CAD consulting.

ECAD

User's manuals for DRACULA, SYMBAD, Parasitic Extractors, LVS and other VLSI CAD tools.

IBM

Hardware and software system design for milling machine-based Numerical Control.

EMPLOYMENT HISTORY

Present-1980: InnerVision Computers: Chief Consultant.
See Sampler of Clients and Projects above.

2000-1990: Teacher

2000-1999: San Jose State University Extension, Teacher/Course Development
1999-1993: Instruction Set, Teacher/Author
1987-1985: Northeastern University, Teacher
1978-1977: Ohlone Junior College, Teacher
1973-1975: Hewlett Packard Corporation (teaching hardware and software)

- Developed and taught courses on at the various institutions listed above on the following topics: Web programming, Perl, CGI, RISC Architecture, Compiler Design, Advanced Logic Design, Intel 8X86 Assembler, Unix System System Administration, Unix for beginners, logic and micro-Processor design
- Authored book anonimously: Programming with Perl and CGI .

1985-1980: National Semiconductor, System Software Advisor

- researched design and development of RISC architecture
- developed front-end for advanced optimizing Pascal compiler
- developed disassembler, linker, and loader for 32000 family
- analyzed the performance of 32000 family
- developed and wrote *Marketing Specifications For System 32000 Development System*
- performed competitive analysis and provided technical marketing expertise
- wrote/presented papers; chaired conference sessions at Wescon, Compcon and others

1980-1978: XEROX Palo Alto Research Center, Member of Research Staff

- defined VLSI processor architecture optimized for MESA language, including BitBlt graphics
- simulated architecture for 32-bit processor design
- designed VLSI NMOS 32K RAM chip (3 Xstor cell)
- developed, implemented, and tested NMOS content addressable memory
- supported SPICE-II circuit simulator (FORTRAN IV)
- investigated development/acquisition of VLSI testers
- developed custom-made purchase order, document tracking system
- developed program for layout of regular LSI structures

1978-1973: Hewlett Packard Corporation, Member of Technical Staff

- developed to completion CPU product (HP300/3000) using CMOS/SOS technology
- designed control section of RALU chip (10,000 transistors)
- designed and documented Bus Interface Controller (BIC)
- developed system micro-diagnostics for RASS chip and BIC
- developed stuck-at-fault tests for fault checking and isolation of BIC
- programmed automatic PLA logic simulator system
- developed PROM burner system
- taught programming and maintenance on 21Mx computer family

EDUCATION AND CREDENTIALS

- BSEE from Cal State University, Long Beach
- Junior College Teaching Credential in Math and Engineering
- Seminars in Speech Recognition, Speech Synthesis, Parallel Processing, MPI programming, and more.

MISCELLANEOUS PROJECTS

- Neural network program for pattern recognition
- Automatic Parser Generator - Table driven parser generator for a compiler front-end
- Parser for Euler Language
- Architect, design and construction of bit-slice RISC mini-computer
- Editor, *49er Engineer Magazine*